# I. Design of Type-I Second order PLL

A type-I second order PLL is shown in Fig 1. The gain ($K_{VCO}$) of the oscillator is 150 MHz/V with center frequency of 1 GHz. The gain of the phase detector ($K_{PD}$) is $\frac{2}{\pi}$ V/rad.

1. Design and Simulate a Type-I Second order PLL for the following cases:-

Case:I Design R and C for $\zeta$ = 0.707.

Case:II Design R and C for $\zeta$= 1.

Case:III Design R and C for $\zeta$=5.

where,

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}, \quad \omega_{LPF} = \frac{1}{RC}$$

In which of the above cases, PLL locks with the reference input faster?

2. Determine the settling time within 2% tolerance for the case I and verify from the simulations.

3. Observe the settling time and steady state phase error for the above three cases in the simulations.

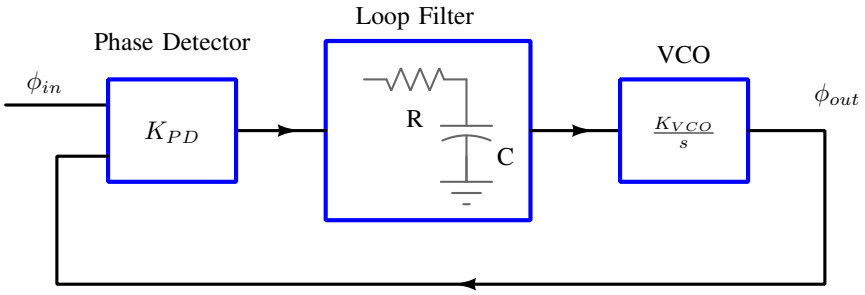


Fig. 1. Type I second order PLL

For PLL simulations using ideal blocks

1). You can use phase detector and VCO blocks from ahdlLib in cadence virtuoso.

2). You should first simulate and verify the phase detector and VCO characteristics before keeping them in the feedback.

3). Use transient analysis to know $K_{PD}$ of the phase detector.

Hints:-

1). The closed loop transfer of second order system is given as:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{1}$$

2). The closed loop transfer of second order PLL is given as:

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_{PD}K_{VCO}}{RCs^2 + s + K_{PD}K_{VCO}} \tag{2}$$

3). Compare Eq. (1) and Eq. (2) ,

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}, \quad \omega_{LPF} = \frac{1}{RC} \tag{3}$$
$$\omega_n = \sqrt{K_{PD}K_{VCO}\omega_{LPF}}$$

4). The settling time within $2\%$ tolerance for $0<\zeta<1$ is given by

$$T_s = \frac{4}{\zeta\omega_n} \tag{4}$$