Lab Assignment: Single Stage Amplifier Design

1. Common source amplifier

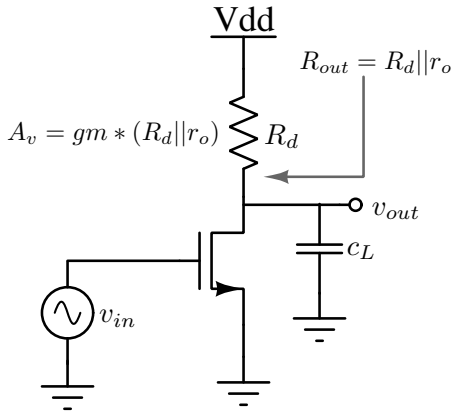

Fig. 1. Common source amplifier with resistive load.

Design a Common source amplifier (as shown in figure) with the following specifications:

$c_L = 5\ pF$

Gain $A_v = 10\ dB$

$P_{dc} = 1\ mW$

BW = 10MHz

Steps:

1. From the design equations, estimate the required g_m and R_d

2. Bias the MOS in saturation at proper current to achieve required g_m (run dc analysis to check MOS biasing condition)

3. Once the MOS is in saturation run AC analysis and check the obtained gain and Bandwidth.

4. Check the output resistance R_{out} and verify whether its value is $R_d||r_o$

5. Tweak the design in case the design requirements are not met.

2. Common Drain amplifier/Source follower

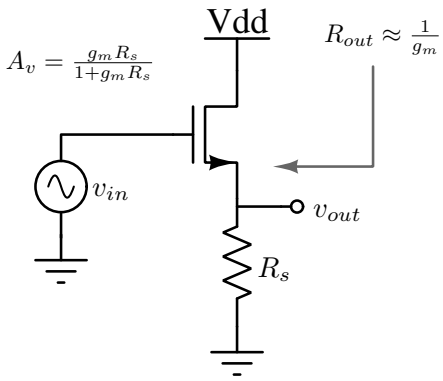

Fig. 2. Common Drain amplifier.

Design a Common drain amplifier to drive a 50 ohm load at the output.

Steps:

1. Bias the MOS in saturation for a g_m of 20 mS.

2. $g_m R_s \gg 1$

3. Check the real part of output resistance R_{out}, it should be equal to 50 Ω

4. Tweak the design in case the design requirements are not met