Chapter 1

Oscillator

1.1 Objective

Q1: Design an NMOS cross-coupled LC oscillator at a frequency of 2.5 GHz
(a) Find out the power consumed by the oscillator
(b) Find out the phase noise at an offset of (*i*) 100 KHz and (*ii*) 20 MHz
Q2: Design a CMOS cross-coupled LC oscillator at a frequency of 2.5 GHz
(a) Find out the power consumed by the oscillator
(b) Find out the phase noise at an offset of (*i*) 100 KHz and (*ii*) 20 MHz
Q3: Compare CMOS and NMOS oscillators in terms of PN, voltage swing, and power dissipation.

1.2 Procedure

Step 1: Tank design - Determine the value of L and C
Choose the value of the inductor:
Larger L → large Rp → increase in amplitude
Larger L → large Rp→ poor Quality factor → poor PN
Use center-tapped inductor and give V_{DD} at the center of the inductor
Find C using

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{1.1}$$

Step 2: Estimate the R_P of the tank using *sp* analysis

Calculate R_P using the equation discussed in the tutorial and verify this by sp analysis (you can neglect the losses in the capacitor)

For *sp* analysis connect port to the tank and open ADE window
Analyses → *ADE L*
From ADE window *Launch* → *Choose*

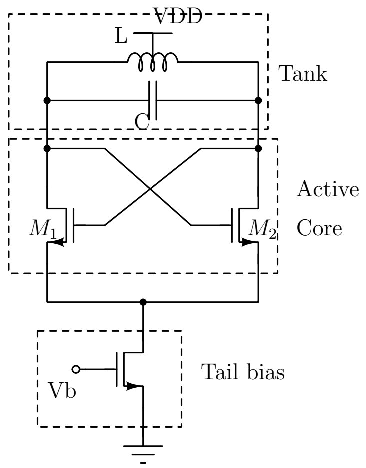

Figure 1.1: Oscillator schematic.

For running simulation
Simulation → Netlist and Run
Plot the results of sp analysis by
Results → Direct Plot → Main Form
Plot Z_{11} and measure R_P
Step 3: Design of active core
Choose both transistors with same g_m (Choose transistor with $f_T \approx 10 f_0$)
For oscillator startup loop gain $> 1 \Rightarrow g_m.R_P > 2$
choose $gm.R_P > 4$
Step 4: Setting transistor width for the required g_m
Run DC analysis to find the g_m of the transistor and adjust the width accordingly for the required g_m
To get the g_m *Results → Print → DC Operating Points*
click on the transistor it will print the g_m
Step 5: Tail bias
Choose the transistor width as high as possible to reduce the flicker noise upconversion from the bias transistor.
Step 6: Transient analysis
Before transient analysis give initial condition at the oscillating nodes
Simulation → Convergence Aids → Initial Condition
Also select the outputs to be plotted
Outputs → To Be Plotted → Select On Design
Now do transient analysis by choosing appropriate stop time

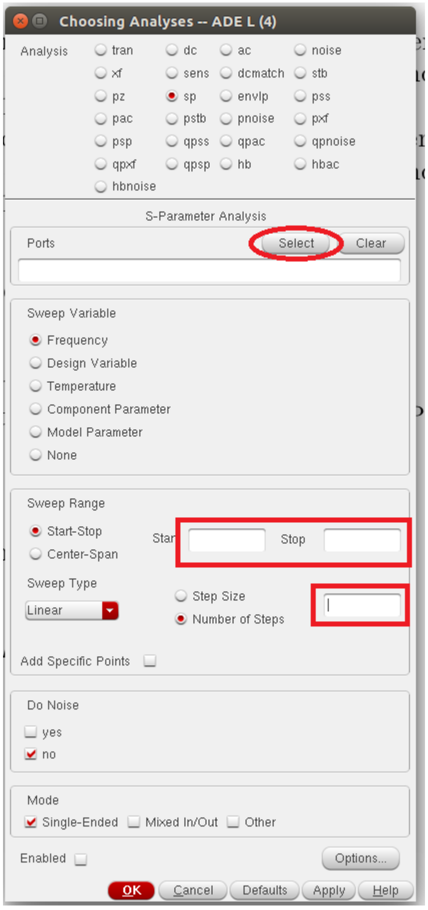

Figure 1.2: sp analysis setup.

From the Visualization and Analisis XL window calculate DFT to find the frequency of oscillations

Step 7: Plotting Phase Noise

PSS and Pnoise analysis to be done for phase noise calculation.

Periodic Steady State setup is below **??**

Write the offset frequency range, where phase noise to be calculated, on the *output frequency sweep range* in the pnoise setup window

To plot phase noise

Results → *Direct Plot* → *Main Form*

Step 8: Run DC analysis and find the current drawn from the V_{DD} and find the power dissipation

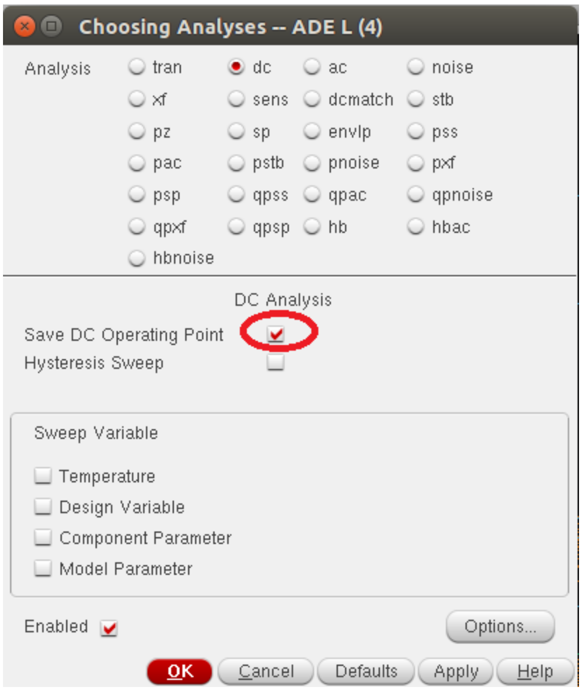

Figure 1.3: DC anaysis setup.

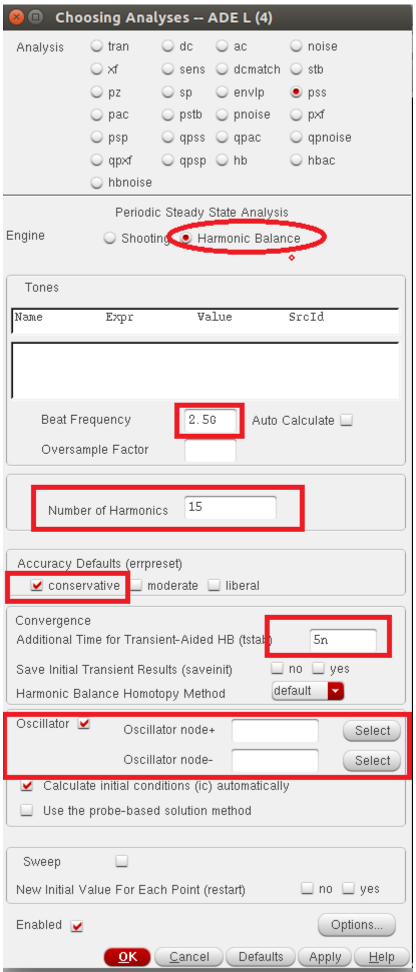

Figure 1.4: pss analysis setup.

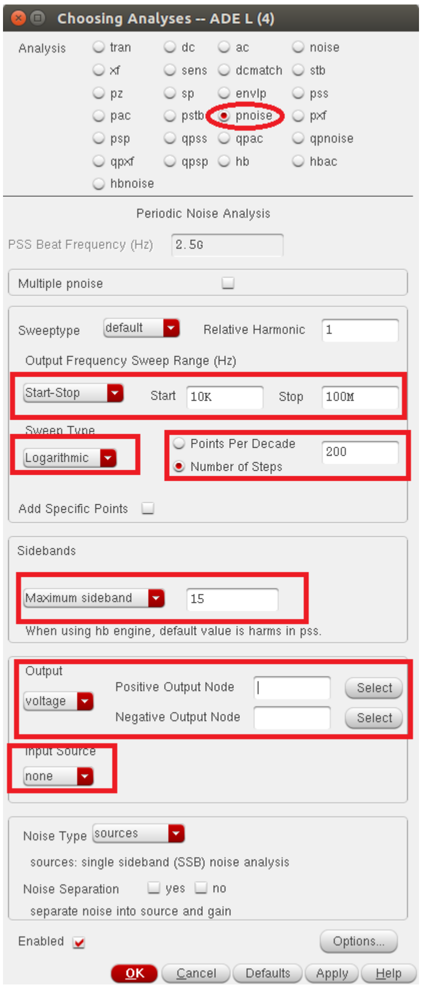

Figure 1.5: pnoise analysis setup.

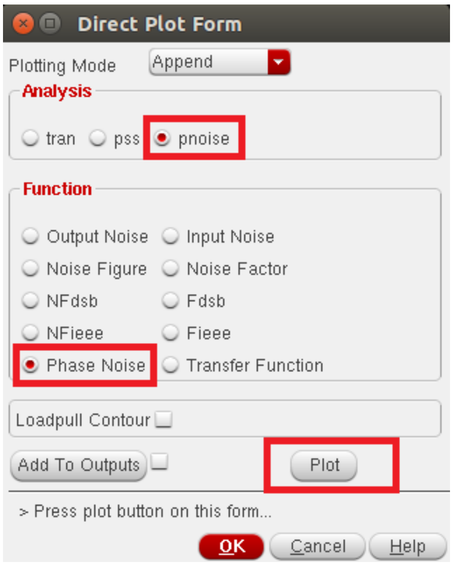

Figure 1.6: Plotting Phase Noise.

CMOS Oscillator

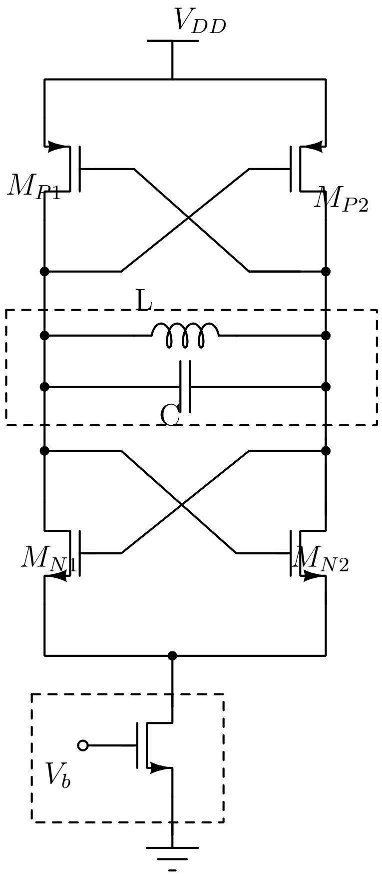

Figure 1.7: CMOS LC Oscillator.

Follow the same procedure, but use a normal inductor (no need center tapped inductor) as V_{DD} is given at the Source of PMOS.

Choose $W_p = 2W_n \rightarrow g_{mp} = g_{mn}$

Oscillator loop gain $> 1 \Rightarrow (g_{mp} + g_{mn}).R_P > 2 \Rightarrow g_m.R_P > 1$

For startup use 2 or 3 times higher loop gain $\Rightarrow g_m.R_P > 2$

Run pss and pnoise analysis and plot phase noise