Design a Class-A power amplifier operating from a 2 V supply with output power P_{out}=20 dBm or 150mW at f_o=1 GHz and determine the following parameters.

- Output power (P_{out} dBm).

- Power added efficiency (PAE %).

- 1 dB compression point (P1dB).

- Third order intercept (IP3).
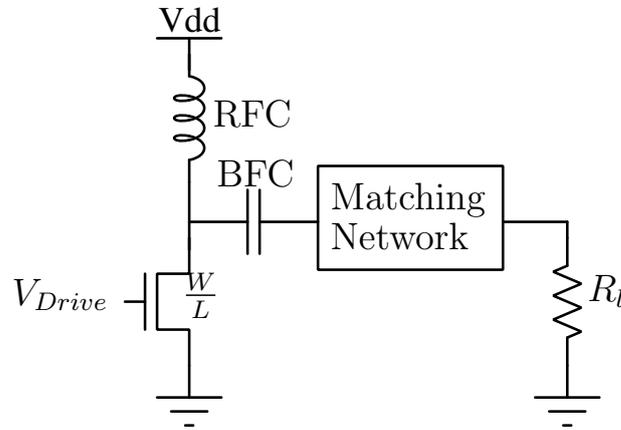
Figure 1: Typical schematic of a CMOS Class-A power amplifier.

$$P_{max} = \frac{V_{dd}^2}{2R_l} \tag{1}$$

Given V_{dd}=2 V and R_l=50 Ω we achieve a P_{out}=40mW ?? 4 times lower than the required 150mW.

Use a matching network to transform the load impedance from R_l=50 Ω to required from P_{max} relation.
Use the following equations for low-pass matching network.

$$Q = \sqrt{\frac{R_l}{R_{in}} - 1} \tag{2}$$

$$C_1 = \frac{Q}{\omega R_l} \tag{3}$$

1
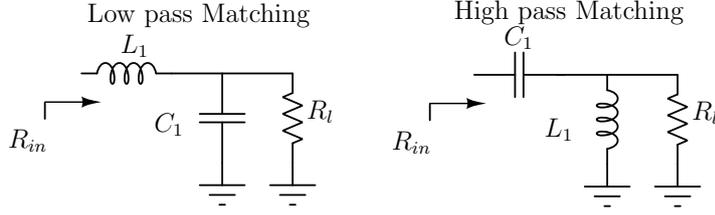
Figure 2: L-match configuration.

$$L_1 = \frac{1}{\omega^2 C_1} \frac{Q^2}{1 + Q^2} \tag{4}$$

and the following for high-pass matching network.

$$Q = \sqrt{\frac{R_l}{R_{in}} - 1} \tag{5}$$

$$L_1 = \frac{R_l}{\omega Q} \tag{6}$$

$$C_1 = \frac{1}{\omega^2 L_1}\left(1 + \frac{1}{Q^2}\right) \tag{7}$$

Design guideline,

- Always transform the load impedance to a value lower than computed, to account for various losses.

- Choose a high-pass or a low-pass matching network with either a parallel or a series resonator.

- Size the width of NMOS transistor for an effective $R_{on} \approx 0.3$ Ω, .

- RFC impedance needs to be atleast 10 times the transformed load impedance $\omega L_{RFC} \approx 10^* R_{in}$, compute L_{RFC} at ω.

- The NMOS is biased in saturation mode, initial point of reference is $\frac{V_{dd}}{2}$.

Perform HB analysis setup with reference to the below screenshots.
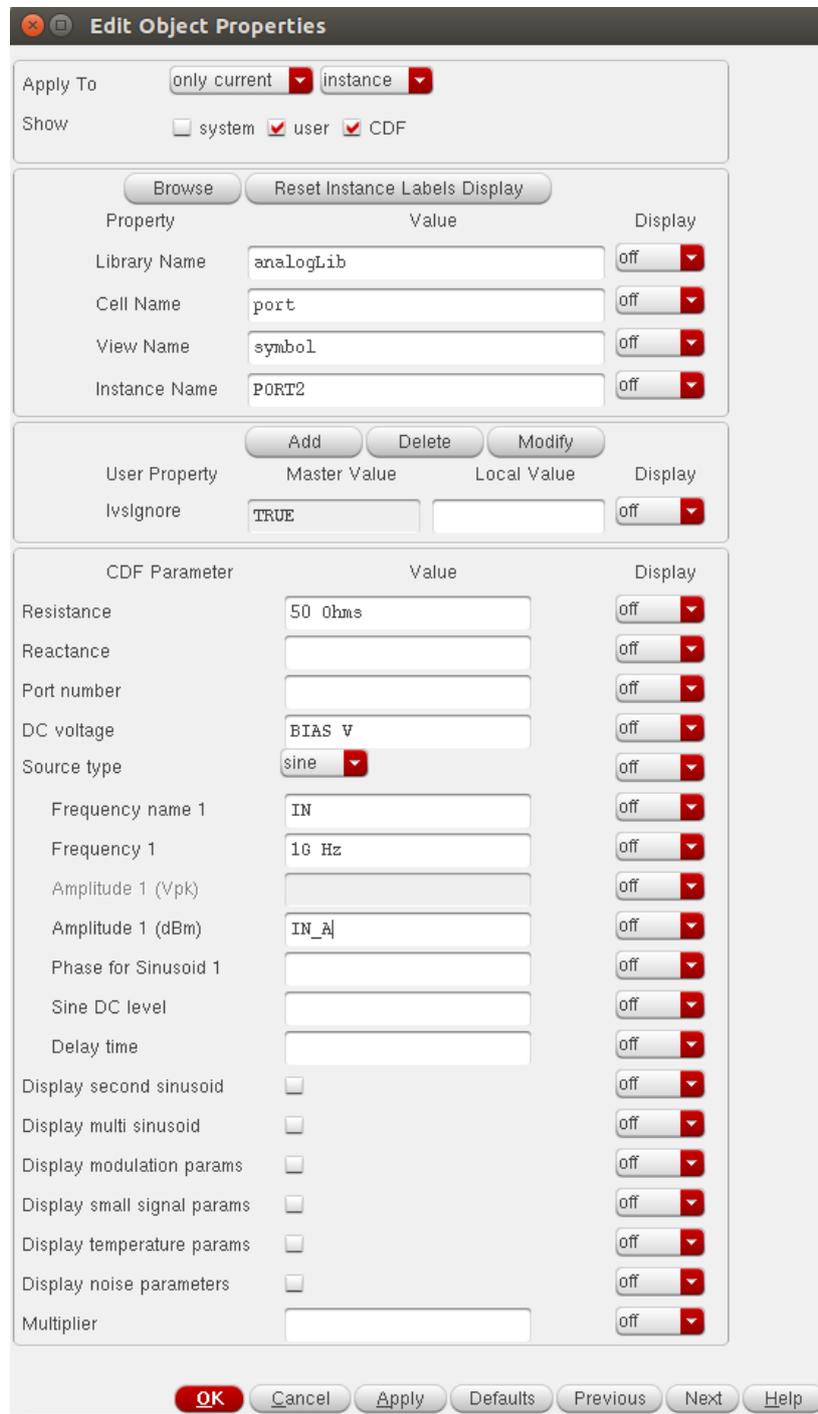
Figure 3: Set the input port parameters as shown.
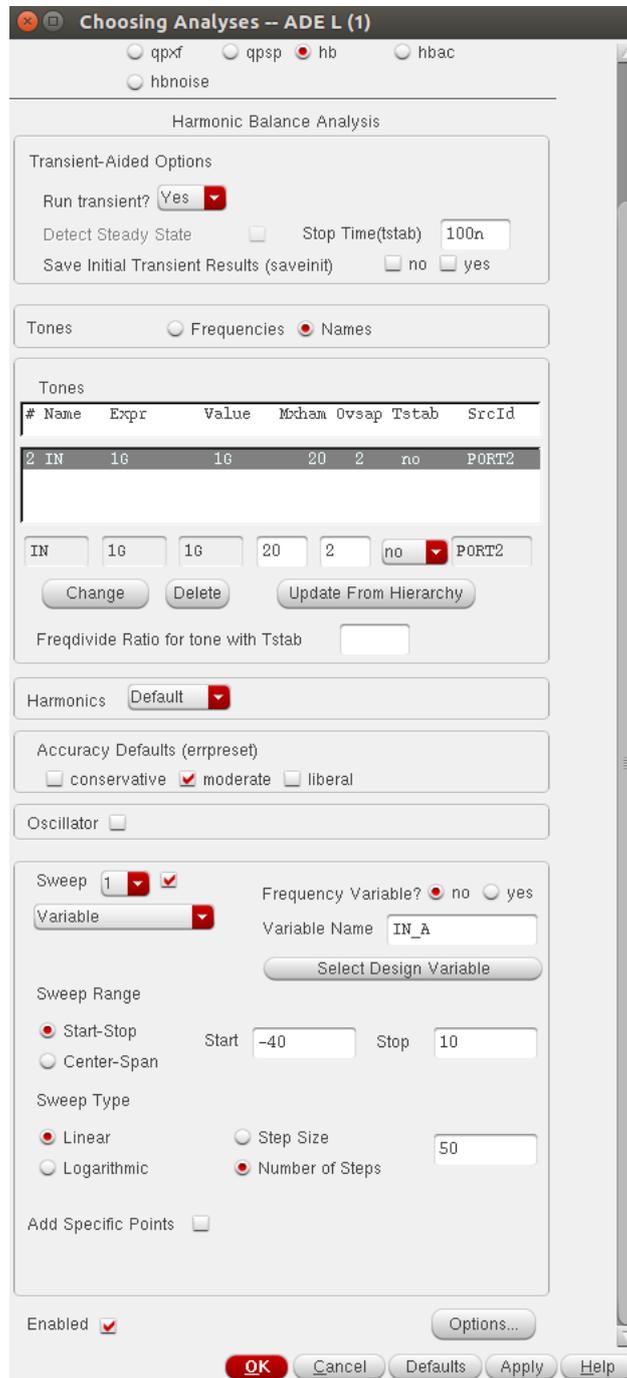
Figure 4: HB setup sweeping the input power from -40dBm to 10 dBm to compute P1dB compression point and IP3.
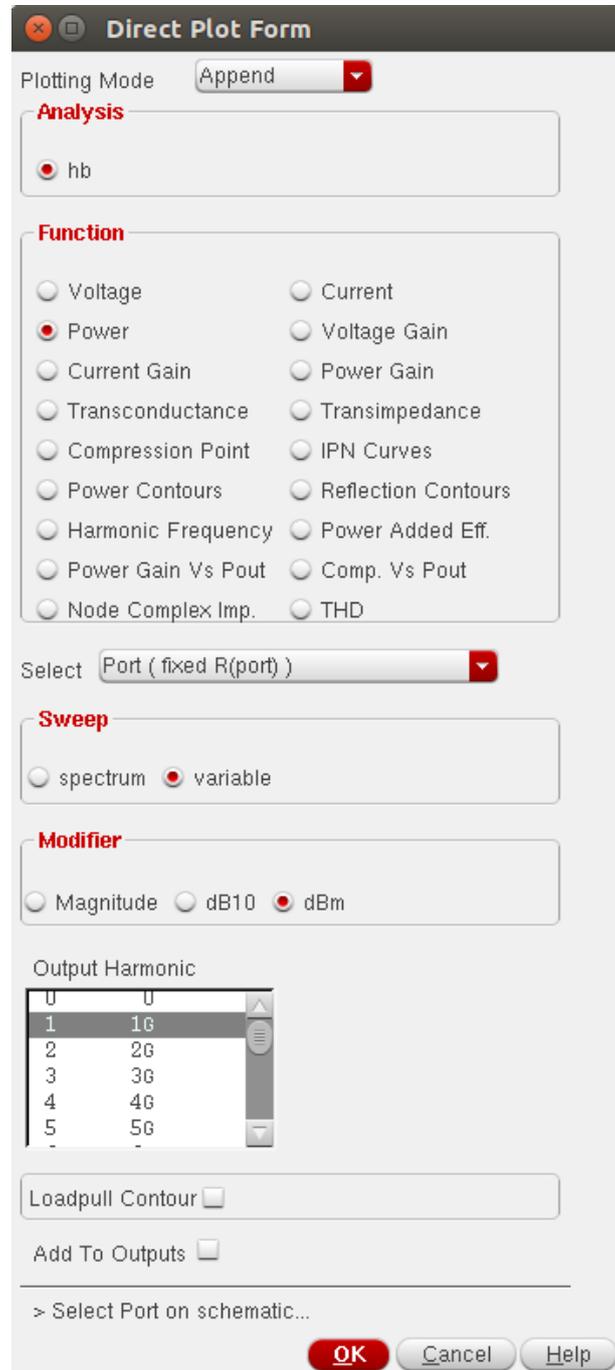
Figure 5: HB form window to plot P_{out}, PAE %, P1dB and IPN .
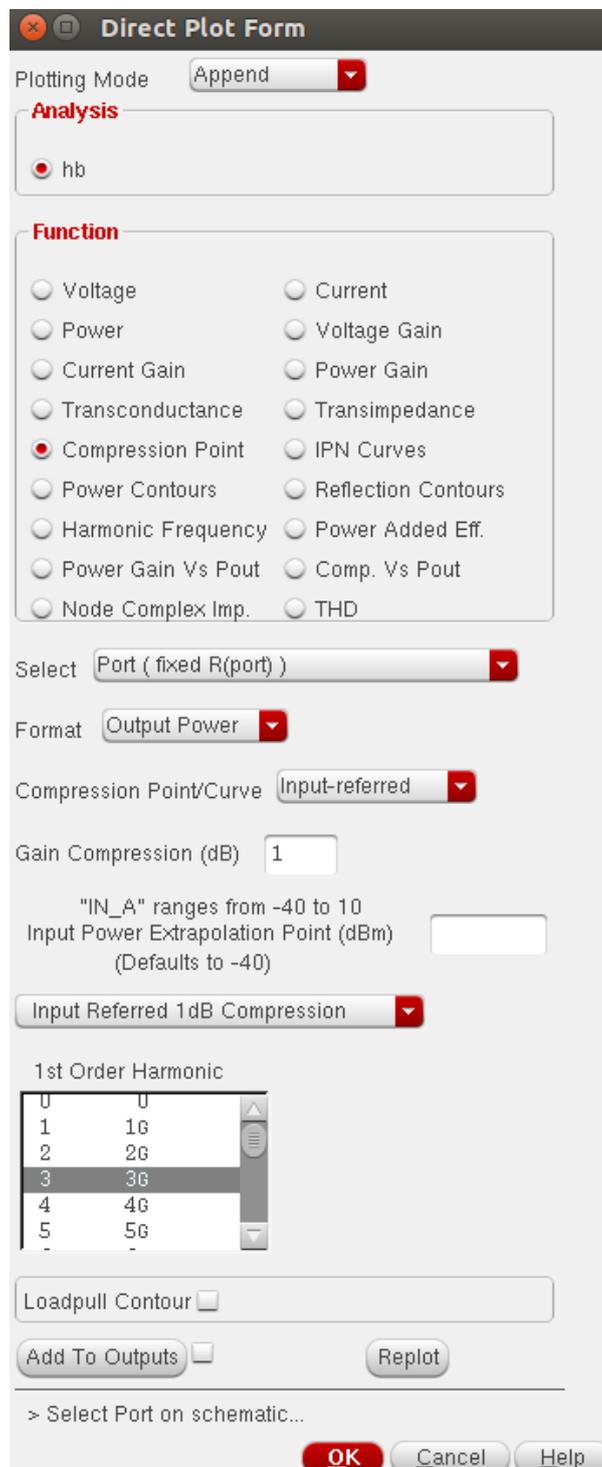
Figure 6: P1dB 1dB compression point.
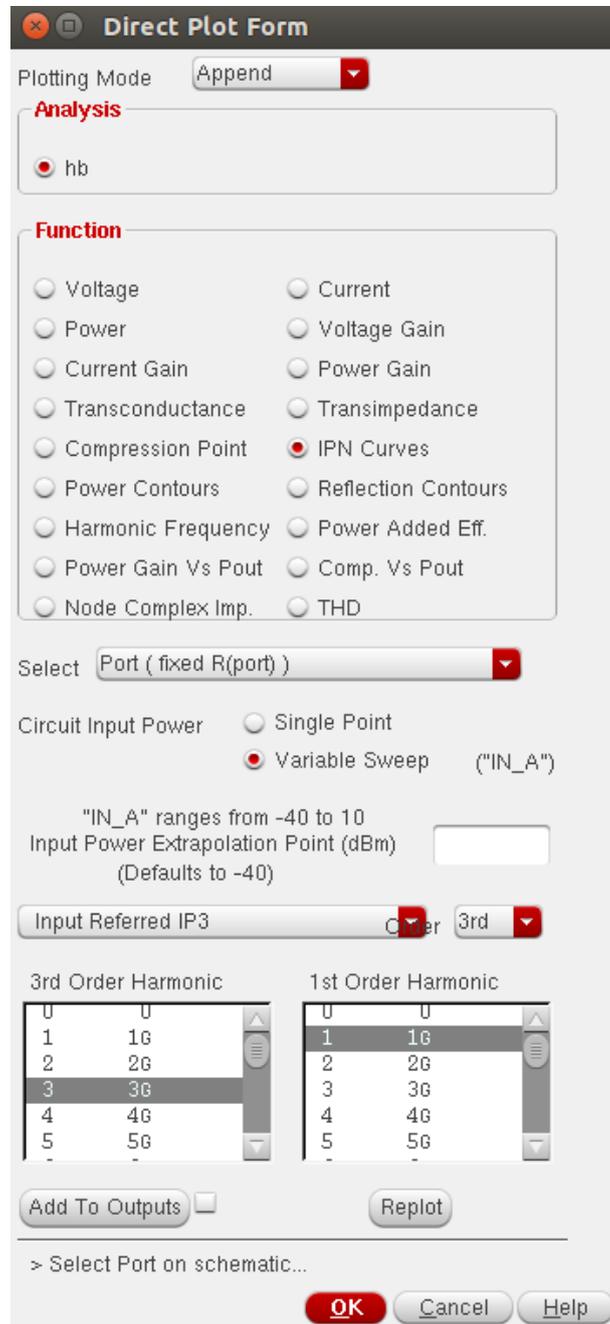
Figure 7: IP3, input power level at which the fundamental and third harmonic have the same power level.